REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-9 are now present in this application. Claim 1 is independent. Claim 1 has been amended. Reconsideration of this application, as amended, is respectfully requested.

Rejection Under 35 U.S.C. § 103

Claims 1 and 3-9

Claims 1 and 3-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,384,279 to Stolmeijer et al. (Stolmeijer) in view of U.S. Patent No. 5,899,732 to Gardner, and claim 2 stands rejected over Stolmeijer and Gardner, and further in view of Takamura. These rejections are respectfully traversed.

Stolmeijer discloses a highly doped silicon substrate 2 (see Stolmeijer, Col. 5, lines 4). Stolmeijer also discloses semiconductor regions 5 and 6. Interposed between the highly doped silicon substrate 2 and adjacent semiconductor regions 5 and 6 is a lesser doped epitaxially grown top layer 3. In other words, the substrate has a *buried layer* beneath the twin wells 5 and 6.

The Applicants have previously argued that the substrate has no buried *implanted* layer beneath the twin wells. In the present Amendment, Applicants

have amended independent claim 1 to delete the limitation "implanted." It is well known in the art that buried layers include both implanted layers and epitaxially grown layers. Epitaxially grown layer 3 of Stolmeijer is a buried layer, though not "implanted" in a general sense. At *http:www.icknowledge.com/glossary/b.html*, a buried layer is defined as a low resistivity doped layer underneath the surface of a semiconductor. Buried layers may be formed by pre deposition - diffusion followed by epitaxial growth, ion implantation and diffusion followed by epitaxial growth or by high energy ion implantation (see enclosed copy). From this well-known definition, it is clear that buried layers include (but are not restricted to) implanted layers.

At *http://www.vtt.fi/ele/results/pdf_files/micro2000.pdf*, it is disclosed that it is possible to utilize an epitaxially grown buried layer in bipolar transistors, and the damage caused by buried layer implantation is eliminated (see enclosed copy). Here, the *epitaxially grown buried layer* is used as an alternative to a buried implanted layer.

The Applicants' claimed invention does not utilize a buried layer, whether it be an implanted layer or an epitaxially grown layer. Particularly, Stolmeijer fails to teach or suggest a combination of elements in a semiconductor device including wherein said substrate has no buried layer beneath the twin wells, as recited in independent claim 1, as amended. Neither Gardner or Takamura can supply the deficiency of Stolmeijer. Reconsideration and withdrawal of these art grounds of rejection are respectfully requested.

With regard to dependent claims 2-9, Applicants submit that claims 2-9 depend, either directly or indirectly, from independent claim 1 which is allowable for the reasons set forth above, and therefore claims 2-9 are allowable based on their dependence from claim 1. Reconsideration and allowance thereof are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachments: *2.4 Deep Trench Isolation of IC Transistors*
Glossary B